

CLAIM LISTING

1. (Currently Amended) An electronic circuit adapted to communicate send a signal to a plurality of two or more additional separate electronic circuits over a common transmission line while simultaneously receiving additional signals from the plurality of two or more additional separate electronic circuits over the common transmission line, the electronic circuit including comprising:
 - (a) signal sending circuitry coupled to an interface node which is adapted to be coupled to the common transmission line, the signal sending circuitry for applying a signal from the electronic circuit to cooperate in creating a combined signal at the interface node, the combined signal being dependent upon on the signal from the electronic circuit and the signals simultaneously applied by the plurality of two or more additional separate electronic circuits connected at other points on to the common transmission line; and
 - (b) decoding circuitry coupled to the interface node, the decoding circuitry for detecting the combined signal at the interface node and decoding the additional signals from the combined signal two or more separate electronic circuits responsive to the combined signal.

- 1 2. (Currently Amended) The electronic circuit of Claim 1 wherein the signal sending
2 circuitry includes comprises:
 - 3 (a) a signal driver; and
 - 4 (b) an encoding element connected between the signal driver and the interface node.
- 5
- 6 3. (Original) The electronic circuit of Claim 2 wherein the encoding element comprises a
7 resistor.
- 8
- 9 4. (Currently Amended) The electronic circuit of Claim 1 wherein the decoding circuitry
10 includes comprises:
 - 11 (a) a first differential receiver having a positive input connected to receive the
12 combined signal and having an a negative input connected to a first reference
13 voltage source.
- 14
- 15 5. (Currently Amended) The electronic circuit of Claim 1 wherein the decoding circuitry
16 includes comprises:
 - 17 (a) a reference voltage multiplexer connected to receive a first digital signal as a
18 control signal, and having second and third reference voltage inputs;
 - 19 (b) a second differential receiver having a positive input connected to receive the
20 combined signal, and a negative input connected to receive an output of the
21 reference voltage multiplexer.
- 22

1 6. (Currently Amended) The electronic circuit of Claim 1 wherein the decoding circuitry
2 ~~includes~~ comprises:

3 (a) an additional reference voltage multiplexer connected to be controlled by a first
4 digital signal and a second digital signal and having fourth, fifth, sixth, and
5 seventh reference voltage inputs; and

6 (b) a third differential receiver having a positive input connected to receive the
7 combined signal and an a negative input connected to receive an output from the
8 additional reference voltage multiplexer.

9
10 7. (Currently Amended) An electronic circuit arrangement ~~including~~ comprising:

11 (a) ~~[[a]]~~ three or more circuits connected together by a common transmission line,
12 each circuit adapted to assert a respective digital signal;

13 (b) each circuit including sending circuitry connected to the common transmission
14 line, the sending circuitry of the respective circuits cooperating to produce an
15 encoded signal on the transmission line based upon the values of the respective
16 digital signals asserted by the respective circuits, the encoded signal comprising
17 one signal from a set of unique encoded signals with each different signal in the
18 set being representative of a particular combination of digital signals asserted
19 simultaneously from the respective circuits; and

20 (c) each circuit further including a decoding arrangement for decoding the encoded
21 signal appearing on the common transmission line to produce the digital signals
22 asserted from each other circuit.

- 1 8. (Original) The electronic circuit arrangement of Claim 7 wherein each circuit is located
2 on a separate integrated circuit chip and the common transmission line comprises a
3 conductor connected to a single electrode on each separate integrated circuit chip.
4
- 5 9. (Original) The electronic circuit arrangement of Claim 7 wherein the signal sending
6 circuitry in each respective circuit includes an encoding element comprising a resistor.
7
- 8 10. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the ~~plurality~~
9 of three or more circuits includes a first circuit providing a first digital signal, a second
10 circuit providing a second digital signal, and a third circuit providing a third digital
11 signal, and wherein the decoding arrangement associated with the second and third
12 circuits includes a first digital signal decoding arrangement comprising:
13 (a) a first differential receiver having a positive input connected to receive the
14 encoded signal and having an a negative input connected to a first reference
15 voltage source.
16
- 17 11. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the ~~plurality~~
18 of three or more circuits includes a first circuit providing a first digital signal, a second
19 circuit providing a second digital signal, and a third circuit providing a third digital
20 signal, and wherein the decoding arrangement associated with the first and third circuits
21 includes a second digital signal decoding arrangement comprising:

- 1 (a) a reference voltage multiplexer connected to receive the first digital signal as a
2 control signal, and having second and third reference voltage inputs;
3 (b) a second differential receiver having a positive input connected to receive the
4 encoded signal, and an a negative input connected to receive an output of the
5 reference voltage multiplexer.
6

7 12. (Currently Amended) The electronic circuit arrangement of Claim 7 wherein the plurality
8 of three or more circuits includes a first circuit providing a first digital signal, a second
9 circuit providing a second digital signal, and a third circuit providing a third digital
10 signal, and wherein the decoding arrangement associated with the first and second circuits
11 includes a third digital signal decoding arrangement comprising:

- 12 (a) an additional reference multiplexer connected to be controlled by the first digital
13 signal and second digital signal, and having fourth, fifth, sixth, and seventh
14 reference voltage inputs; and
15 (b) a third differential receiver having a positive input connected to receive the
16 encoded signal and an a negative input connected to receive an output from the
17 additional reference voltage multiplexer.
18

19 13. (Currently Amended) An electronic system having a first circuit producing a first digital
20 signal, a second circuit producing a second digital signal, and a third circuit producing a
21 third digital signal, the system including comprising:

1 (a) a first circuit encoding element included in the first circuit, a second circuit
2 encoding element included in the second circuit, and a third circuit encoding
3 element included in the third circuit, each respective encoding element connected
4 between a digital signal output of the respective circuit and a common
5 transmission network between the first, second, and third circuits, the first,
6 second, and third encoding elements cooperating to produce an encoded signal on
7 the common transmission network based upon the values of the first, second, and
8 third digital signals, the encoded signal comprising one signal from a set of unique
9 encoded signals with each different signal in the set being representative of a
10 particular combination of the first, second, and third digital signals; and

11 (b) a first circuit decoding arrangement included with the first circuit, a second circuit
12 decoding arrangement included with the second circuit, and a third circuit
13 decoding arrangement included with the third circuit, the respective decoding
14 arrangement for each respective circuit for decoding the encoded signal to
15 produce the digital signals produced by each other circuit in the system.

16
17 14. (Original) The electronic system of Claim 13 wherein the encoding elements each
18 comprise a resistor.

- 1 15. (Currently Amended) The electronic system of Claim 13 wherein the first circuit
2 decoding arrangement includes comprises:
- 3 (a) a reference voltage multiplexer connected to be controlled by the first digital
4 signal and connected to receive second and third reference voltage signals as
5 inputs;
- 6 (b) a second differential receiver having a positive input connected to receive the
7 encoded signal and a negative input connected to receive a reference voltage
8 multiplexer output;
- 9 (c) an additional reference voltage multiplexer connected to be controlled by the first
10 digital signal and the second digital signal, and connected to receive fourth, fifth,
11 sixth, and seventh reference voltage signals as inputs; and
- 12 (d) a third differential receiver having a positive input connected to receive the
13 encoded signal and a negative input connected to receive an output of the
14 additional reference voltage multiplexer.
- 15
- 16 16. (Currently Amended) The electronic system of Claim 13 wherein the second circuit
17 decoding arrangement includes comprises:
- 18 (a) a first differential receiver having a positive input connected to receive the
19 encoded signal and a negative input connected to receive a first reference voltage
20 signal;

- 1 (b) an additional reference voltage multiplexer connected to be controlled by the first
2 digital signal and the second digital signal, and connected to receive fourth, fifth,
3 sixth, and seventh reference voltage signals as inputs; and
4 (c) a third differential receiver having a positive input connected to receive the
5 encoded signal and a negative input connected to receive an output of the
6 additional reference voltage multiplexer.

7
8 17. (Canceled)

9
10 18. (New) The electronic system of Claim 13 wherein the third circuit decoding arrangement
11 comprises:

- 12 (a) a first differential receiver having a positive input connected to receive the
13 encoded signal and a negative input connected to receive a first reference voltage
14 signal;
15 (b) a reference voltage multiplexer connected to be controlled by the first digital
16 signal and connected to receive second and third reference voltage signals as
17 inputs; and
18 (c) a second differential receiver having a positive input connected to receive the
19 encoded signal and a negative input connected to receive an output of the
20 reference voltage multiplexer.